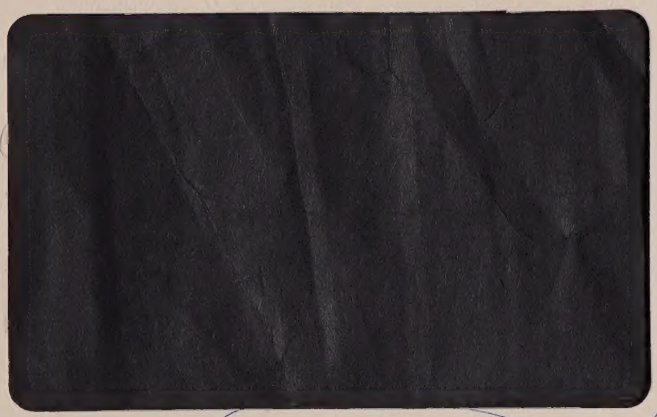
Pulse Instruments



VIKING LABS / HONEYWELL
370 BERNARDO AVENUE
MOUNTAIN VIEW, CA 94043

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED

PULSE INSTRUMENTS COMPANY

USER'S REFERENCE MANUAL

MODEL PI-100A

4-CHANNEL CLOCK GENERATOR

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ±	CONTRACT NO.	PULSE INSTRUMENTS CO. SAN PEDRO, CALIFORNIA 90732	
	APPROVALS / DATE		
MATERIAL	DRAWN		
	CHECKED		
FINISH		SIZE A	CODE IDENT NO.
DO NOT SCALE DRAWING		SCALE	DRAWING NO. 91000040
			SHEET 1 OF

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-1581

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GENERAL DESCRIPTION

The PI-100A 4-channel 50Mhz Clock Generator is a plug-in unit designed to operate in the Tektronix TM-500 series Power Modules. It is compatible with other Pulse Instruments and Tektronix TM-500 series plug-ins operating in standard (non-custom wired) power modules*.

The PI-100A is designed primarily for simplifying timing set-ups in device and circuit testing applications where several synchronized pulse generators are required. When TTL drive levels only are needed, the PI-100A can replace four conventional pulse generators and eliminate cluttering interconnecting cables and Tee connectors normally required for synchronizing pulse generators. In fact, the PI-100A is equivalent to the timing and control portions of four synchronized pulse generators, all packaged into one compact unit.

Master Clock A generates clock periods which are variable from 20ns to 2ms, and it can be synchronously gated to produce pulse bursts. In the external triggering mode, Clock A can be triggered from a single pulse to pulse repetition rates up to 50Mhz. The output pulse width of Clock A is normally fixed at less than $\frac{1}{2}$ the selected period range setting and can be increased to greater than 5 times the range setting when the WIDTH-pull switch is activated.

The outputs of channels B, C and D can each be delayed from less than 10ns to greater than 1ms with respect to that of channel A. The output pulse widths of these channels are variable from less than 10ns to greater than 1ms, and the output polarities can be inverted when the INVERT-pull switch is activated.

The 2V, min. 50 ohm outputs are suitable for driving TTL circuits at the end of a length of 50 ohm cable without the need for 50 ohm load termination.

* Do not force plug-in unit into non-compatible custom wired power modules (identified by non-matching barriers on edge connector inside power modules).

CAUTION

Turn the power module off before inserting the plug-in unit; otherwise, damage may occur to the plug-in circuitry.

SIZE	CODE IDENT NO.	DRAWING NO.
		91000040
SCALE		SHEET 2

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SPECIFICATIONS

MASTER CLOCK "A" PERIOD	⩽ 20ns (50MHz) to > 2ms (500Hz) in five decode steps, plus 10 to 1 continuously variable control. Period jitter < 0.1% of setting +50ps. Active low input connected to $\overline{\text{CLOCK INHIB}}$/EXT CLOCK IN BNC connector (I_{IL} ⩽ 3.2mA) disables Master Clock; +2V min. or open circuit restores free running mode of Clock A.
"B", "C", AND "D" DELAYS (At 1.5V level)	< 10ns to > 1ms in five decade steps, plus 10 to 1 continuously variable control. Delay jitter < 0.1% of setting +50ps.
"A" WIDTH Internal Clock (At 1.5V level)	Fixed at ⩽ $\frac{1}{2}$ of selected period range setting or variable to > 5 times the range setting when WIDTH-pull switch is activated.
External Triggering	⩽ 10ns to > 100ns. 10ns min. width may increase to 11ns max. when clock period is less than 25ns. Width jitter<0.1% of setting +50ps.
"B", "C", AND "D" WIDTHS (At 1.5V level)	⩽ 10ns to > 1ms in five decade steps plus 10 to 1 continuously variable control. 10ns min. width may increase to 11ns max. when clock period is less than 25ns. Width jitter < 0.1% of setting +50ps.
DELAY/WIDTH DUTY FACTORS	⩾ 70% for periods ⩾ 200ns and reduce to 50% at 20ns period.
OUTPUTS, FRONT PANEL	2V min. from 50Ω. t_r, t_f ⩽ 7ns into 50Ω. Normal or inverted outputs on channels B, C, and D. Aberrations ⩽ ±5% with 50Ω termination.
OUTPUTS, REAR EDGE CONNECTOR	16 50Ω Buffered ECL outputs for driving up to four plug-in units.
EXTERNAL TRIGGER INPUT	2V, 10ns pulse width min. into 1KΩ. DC to 50MHz. Trigger input to Master Clock A output delay ⩽ 45ns.

SIZE	CODE IDENT NO.	DRAWING NO. 9100040
SCALE		SHEET 3

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FRONT PANEL CONTROLS

1. PERIOD Upper Range Selector Switch - Selects upper range of Master Clock A period, 20ns, 200ns or 2us.

2. EXT. CLOCK/INT CLOCK INHIBIT Input - Accepts TTL compatible (2-5V) input for triggering Clock A in EXT mode and for inhibiting or gating Clock A in INT mode. A low input disables Clock A in INT mode; +2V min. or open circuit restores free running mode of Clock A.

3. POWER - indicates power is on.

4. PERIOD Lower Range Selector Switch - Selects lower range of Master Clock A period, 20us, 200us or OFF. Upper and lower range settings are additive.

5. MASTER CLOCK A OUTPUT - 2V min. from 50 ohm source, suitable for driving TTL circuits at the end of a length of 50 ohm cable.

6-8 CH.'s B, C & D OUTPUTS - Outputs characteristics similar to those of Clock A.

9. CH. B WIDTH Lower Range Selector Switch - Selects lower range of Ch. B. Output pulse width, 10us, 100us or OFF. Range switches in Ch.'s C and D are identical.

10. CH. B DELAY Lower Range Selector Switch - Selects lower range of Ch. B output delay with respect to that of Ch. A, 10us, 100us or OFF. Range switches in Ch.'s C and D are identical.

11. CH. B. WIDTH Upper Range Selector Switch - Selects upper range of Ch. B output pulse width, 10ns, 100ns or 1us. Settings in upper and lower ranges are additive.

12. CH. B DELAY Upper Range Selector Switch - Selects upper range of Ch. B output delay with respect to that of Ch. A, 10ns, 100ns or 1us. Settings in upper and lower ranges are additive.

13. Continuous DELAY Control - Provides greater than 10 to 1 delay variation in any given range setting.

14. Continuous WIDTH Control/INVERT switch - Provides greater than 10 to 1 width variation in any given range setting. Inverts output polarity when INVERT-pull switch is activated.

15. IN/EXT Selector Switch - Selects internal free running or external triggering mode of Master Clock A.

16. Continuous PERIOD Control - Provides greater than 10 to 1 period variation in any given setting.

17. CH. A Continuous WIDTH Control - Provides greater than 10 to 1 width variation in any given period range setting when WIDTH-pull switch is activated. When WIDTH switch is pushed in, Width A is fixed and is less than or equal to one-half of the selected period range setting.

SIZE	CODE IDENT NO.	DRAWING NO.
		91000040
SCALE		SHEET 4

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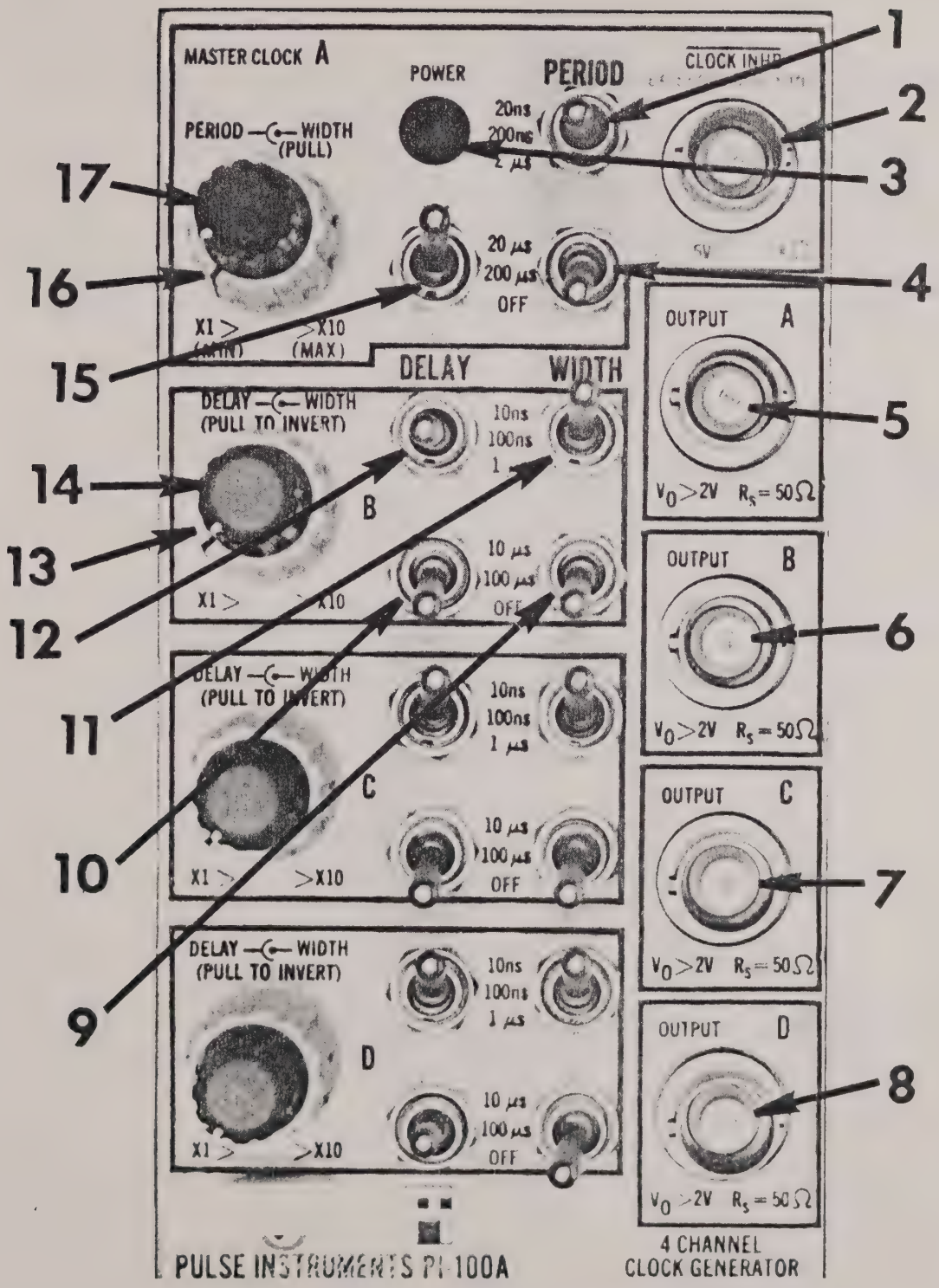
REORDER NO. 20501


MASTER CLOCK A
POWER
PERIOD
CLOCK INHIB
20ns
200ns
2 µs
PERIOD — WIDTH (PULL)
20 µs
200 µs
OFF
X1 >
>X10
(MIN)
(MAX)
DELAY
WIDTH
DELAY — WIDTH (PULL TO INVERT)
10ns
100ns
1
B
10 µs
100 µs
OFF
C
1 µs
D
OUTPUT A
OUTPUT B
OUTPUT C
OUTPUT D
V_0 >2V R_s = 50Ω
PULSE INSTRUMENTS PI-100A
4 CHANNEL
CLOCK GENERATOR
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V. PERFORMANCE CHECK/CALIBRATION PROCEDURE

INTRODUCTION

The only internal adjustment needed for the PI-100A is a variable capacitor for the 20ns period (50 MHZ repetition rate) trim. A selected fixed capacitor, instead of the trimmer, is used for earlier units with Serial Numbers up to #110. Power supply values and other critical parameters are set using precision components. Consequently, no calibration, except for the 20ns period adjustment, will be required. The following tests are recommended to ensure proper operation of the unit when it is received.

TEST EQUIPMENT

The following equipment and accessories are required for checking the PI-100A. Special fixtures, when specified, are used mainly for simplifying the test setup and procedure. They are available from Pulse Instruments.

Dual Channel, 75 MHZ oscilloscope with delaying sweep time base
Dual Channel sampling scope with t_r less then 1ns
50 MHZ pulse generator, Pulse Instruments PI-100A or equivalent
250 MHZ counter/timer, Tektronix DC 505A or equivalent
3½ digit DVM
BNC TEE connector (2)
50 ohm feed-through termination (2)
50 ohm coaxial cable, (4) 3ft length, (1) 6ft length

WARM-UP

Allow the unit to operate in a TM-500 series mainframe for approximately 10 minutes before checking and calibrating it.

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1.14 Decrease the range setting of each function in each channel by one decade, and repeat measurements for all ranges except the last range. All readings shall be less than the corresponding front panel setting values.

Note: Decrease the time base setting in the oscilloscope, and increase the value of N in the counter/timer as needed for obtaining optimum reading.

2. CHECK PERIOD/DELAY/WIDTH @ > X10 Setting (Low Frequency)

2.1 Set all controls to the FCW positions and pull out "A" switch.

2.2 Check for greater than 2us period, and greater than 1us delay and width.

3. CHECK INVERT FUNCTION FOR CHANNELS B, C AND D.

3.1 Pull out invert switch in each channel and check for inversion of outputs B, C and D.

3.2 Push in "A" width and "B", "C" and "D" invert switches.

4. CHECK PERIOD JITTER

4.1 Set period range switches to 200us and 2us.

4.2 Set all delay and width range switches to 100us and 1us.

4.3 Set main time base to 2ms/DIV and obtain a dual waveform display of Clock A and Clock B outputs. The trailing edge of Clock A output and the leading edge of Clock B output should approximately coincide.

4.4 Set delayed time base to 2μs/DIV, intensified, and adjust DELAY TIME multiplier until the intensified portion of the display occurs on the leading edge of the second cycle of the Clock A output (usually occurring at the second vertical line or 4ms position).

4.5 Switch to the delayed time base display mode, and adjust DELAY TIME multiplier slightly until the leading edge of Clock A output is at the center of the screen.

4.6 Check for less than 2us (1 major division) of period jitter (horizontal movement of the display within a time interval of 1 second or less).

Note: Depending on the scope used, a hood may be necessary in order to view the very dim display.

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8. CHECK MIN DELAY AND PULSE WIDTH (Use a sampling scope for checks in 8-12A)

8.1 Set period control to approximately the mid position.

8.2 Connect Clcok A and Clcok B outputs to a dual channel sampling scope using (2) 3ft length 50 ohm cables. (Be sure that the connections to the counter/timer are disconnected).

8.3 Check for less than 10ns delay between the leading edges of the two waveforms, measured at the 0.75Vlevel.

8.4 Check for less than 10ns pulse width for both Clock A and Clock B outputs measured at the 0.75V level.

8.5 Repeat delay and pulse width checks for Clock C and Clock D outputs.

9. CHECK MIN OUTPUT AMPLITUDE

9.1 Adjust pulse width of each channel to ≥ 10ns at the 0.75V level.

9.2 Check for greater than 1V output (this corresponds to 2V min open circuit output).

10. CHECK OUTPUT RISE AND FALL TIMES

10.1 Adjust pulse width of each output to approximately 50ns.

10.2 Adjust scope vertical gain control to obtain a display of 5 divisions.

10.3 Check for less than or equal to 7ns t_r and t_f measured at the 10%-90% points.

11. CHECK EXT. TRIGGERING

11.1 Set INT/EXT switch in Master Clock A to EXT.

11.2 Apply a 2V, 10ns wide pulse to the external clock in BNC connector. (Another PI-100A may be used as the triggering source).

11.3 Set all controls to the FCCW position and all range switches to their min positions.

11.4 Check for 50 MHZ min outputs in Channels A, B, C and D.

12. CHECK EXT CLOCK IN TO A OUTPUT DELAY (Method I, a pulse generator with 2.4V into 50 ohm required).

12.1 Connect a BNC TEE to the EXTERNAL CLOCK IN BNC connector of the PI-100A.

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12.2 Connect the input clock source to one end of the BNC Tee using a 3ft length 50 ohm cable.

12.3 Connect the other end of the BNC TEE to the sampling scope using another 3ft length 50 ohm cable.

12.4 Connect Clock A output to the second channel of the scope input with a 3 ft length 50 ohm cable.

12.5 Adjust input clock source amplitude to approximately 2.4V.

12.6 Check for less than 45ns delay between the leading edges of the waveforms.

12A. CHECK EXT CLOCK IN TO A OUTPUT DELAY (Method II, a second PI-100A required).

12A.1 Connect Clock B output of the driving PI-100A to the external clock in BNC connector of the driven PI-100A using a 3ft length 50 ohm cable.

12A.2 Connect Clock C output of the driving PI-100A to the sampling scope using a 6ft length 50 ohm cable.

12A.3 Connect Clock A output of the driven PI-100A to the second channel of the sampling scope using a 3ft length 50 ohm cable.

12A.4 Set delays of Clock B and Clock C of the driving PI-100A to 10ns, X1. (Typical delay skew among Clocks B, C and D at min setting is 2ns).

12A.5 Check for less than 45ns delay between the leading edges of the waveforms.

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SIZE	CODE IDENT NO.	DRAWING NO.
SCALE		SHEET

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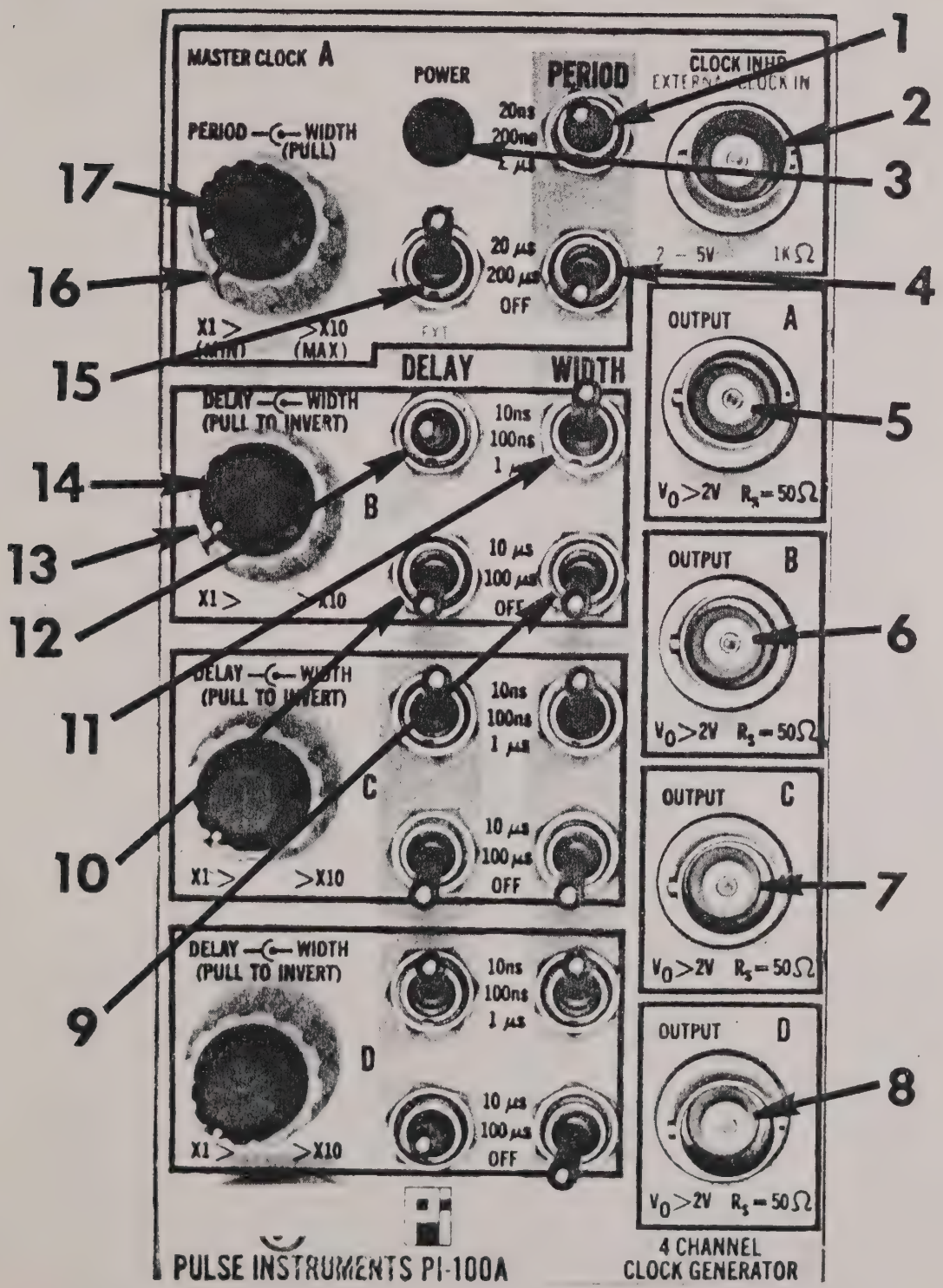
MASTER CLOCK A
POWER
PERIOD
CLOCK INHIB
EXTERNAL CLOCK IN
PERIOD — WIDTH (PULL)
20ns
200ns
2 µs
2 – 5V
1KΩ
20 µs
200 µs
OFF
X1 >
>X10
(MIN)
(MAX)
EXT
DELAY
WIDTH
DELAY — WIDTH (PULL TO INVERT)
10ns
100ns
1 µs
10 µs
100 µs
OFF
B
C
D
OUTPUT A
OUTPUT B
OUTPUT C
OUTPUT D
V_0>2V R_s=50Ω
PULSE INSTRUMENTS PI-100A
4 CHANNEL CLOCK GENERATOR
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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	VALUE CHANGES AT C_{61}, C_{70}, C_{51}, C_{69}, L_8, L_{11}	6-12-78	
B	TOOK OUT R_{96}, 121K, R_{133}, 121K.	10-30-78	
C	VALUES ADDED AT U_6, U_7, U_8, U_9,	2-15-79	

"C" DELAY GENERATOR

"C" WIDTH GENERATOR

"B" DELAY

"D" WIDTH GENERATOR

(E) TO DELAY "C" ANALOG SWITCH NETWORK PG. 4.

Q_{50} - Q_{54} ARE PART OF U_6 CA-3083

(F) TO WIDTH "C" ANALOG SWITCH NETWORK PG. 4.

Q_{55} - Q_{59} ARE PART OF U_7 CA-3083

(G) TO DELAY "D" ANALOG SWITCH NETWORK PG. 4.

Q_{65} - Q_{69} ARE PART OF U_8 CA-3083

(H) TO WIDTH "D" ANALOG SWITCH NETWORK PG. 4

Q_{76} - Q_{80} ARE PART OF U_9 CA-3083

NOTES: 1. ALL CR ARE IN914 UNLESS OTHERWISE SPECIFIED.

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN	1-31-78
CHECKED	

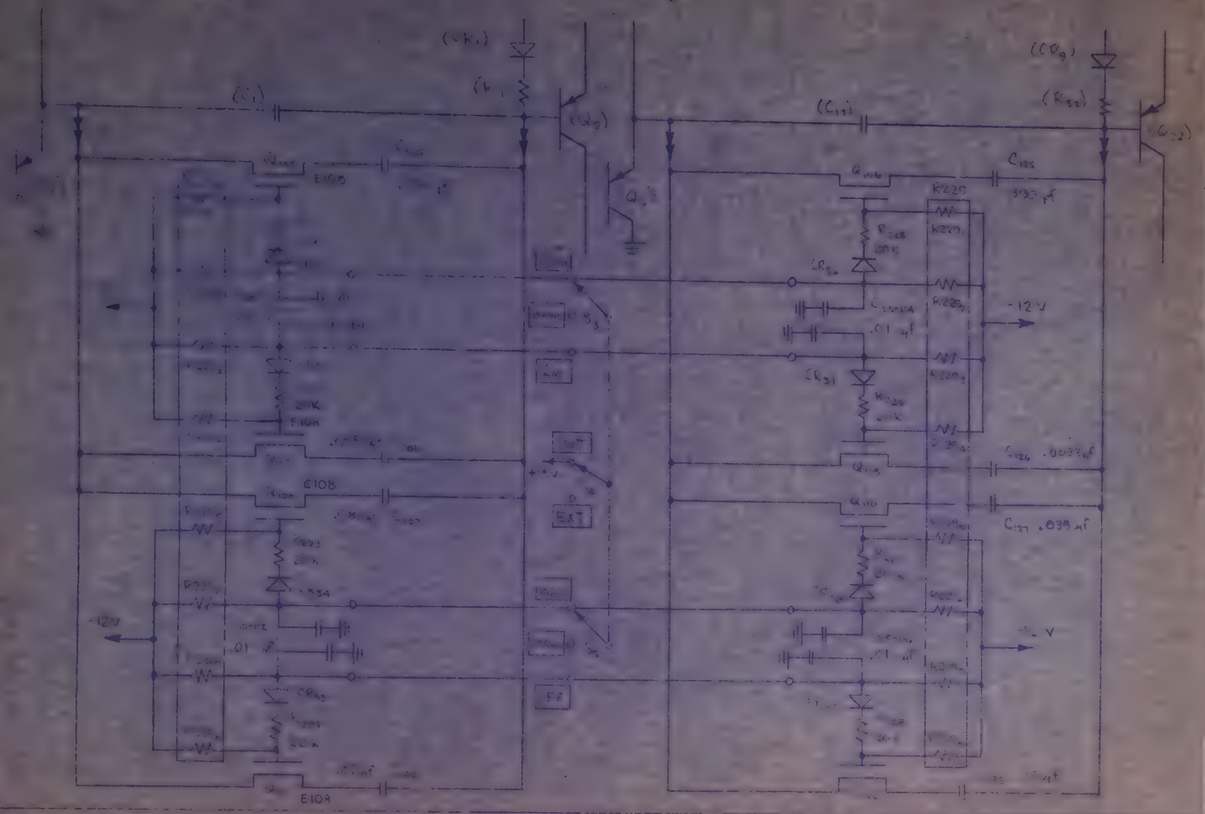
PULSE INSTRUMENTS CO.
SAN PEDRO, CALIFORNIA 90732

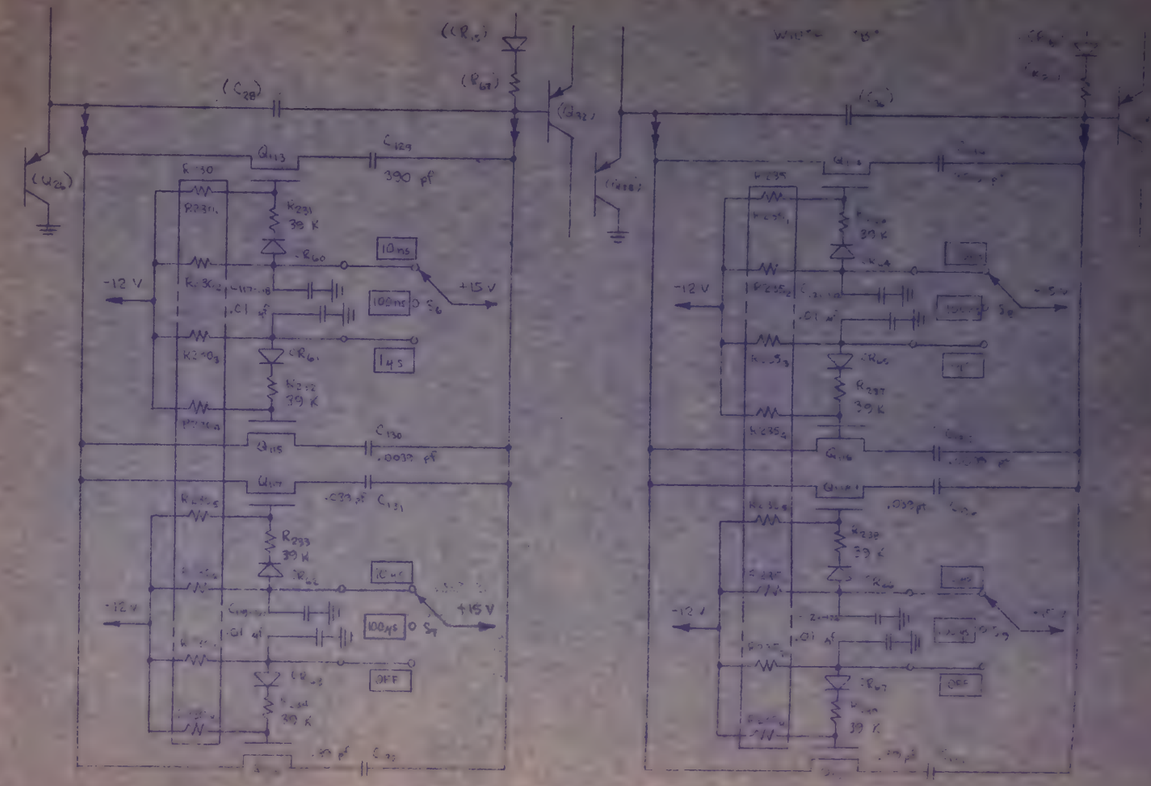
PI-100 4 CHANNEL CLOCK GENERATOR
"C" AND "D" DELAY GENERATORS
"C" AND "D" WIDTH GENERATORS

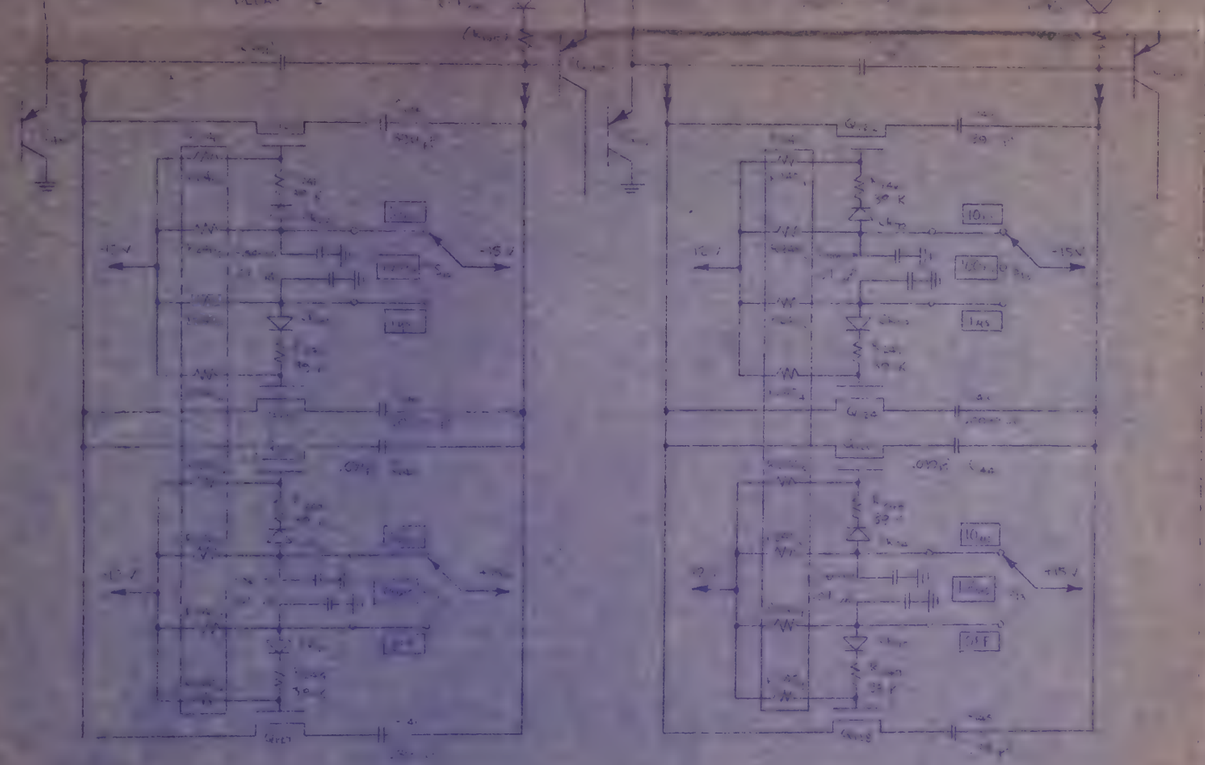
SCALE	SIZE	DRAWING NO.
	C	[illegible]

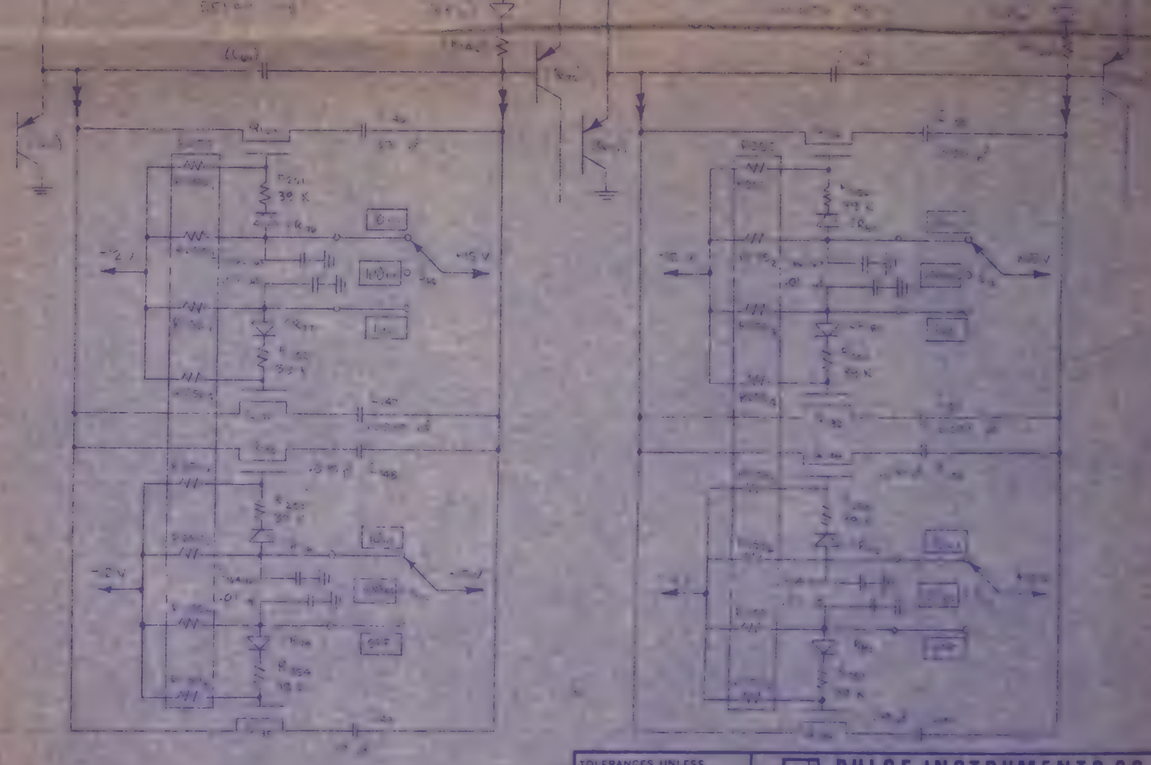
DO NOT SCALE DRAWING | SHEET

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NOTE 3 AND E109 DESIGNATION ADDED	2-25-70	









NOTES:
1. [illegible]
2. [illegible]
3. ALL FET SYMBOLS ARE TOP VIEW AS NOTED

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	.x ±	±

APPROVALS	DATE
DRAWN	
CHECKED	

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SAN PEDRO, CALIFORNIA 90732

[illegible] DELAY METHODS

SCALE	SIZE	DRAWING NO.
	C	[illegible]

DO NOT SCALE DRAWING | SHEET [illegible]

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	[illegible] AT C_{89}, C_{96}, R_{146}.	9-1-78	[illegible]
B	ADDED C_{165} - C_{168}, .01 µF, FROM +5V TO GROUND	10-30-78	
C	VALUE CHANGES AT R_{178}, R_{175}, R_{198}.	11-13-78	
D	WAS C_{165} - C_{168}, IS C_{181} - C_{184}.	11-14-78	
E	ADDED VALUES AT U_{16}, U_{17}	2-15-79	

+5V

390Ω RESISTOR NETWORK

47Ω RESISTOR NETWORK

LOCATED ON MAINFRAME

+5.2V

R_{204} 100Ω

R_{203} 10Ω

C_{88} .01µF

C_{89} 33µF

R_{205} 10Ω

MPQ-6001

Q_{87} - Q_{89} ARE PART OF U_{16} MPQ-6001

+4.5V

R_{186} 5.1Ω

R_{185} 475Ω

Q_{86} 2N3640

R_{184} 15Ω

C_{91} .01µF

R_{183} 6.19Ω

Q_{85} MPS 3640

R_{182} 5.1Ω

R_{180} 475Ω

"A" OUT

"B" OUT

LOCATED ON MAINFRAME

Q_{98} - Q_{101} ARE PART OF U_{17} MPQ-6001

+5.2 V

C_{94} .01µF

R_{203} 10Ω

C_{93} 33µF

R_{204} 100Ω

C_{92} .01µF

+15 V

C_{100} .01µF

R_{205} 10Ω

R_{218} 6.19 K

MPQ6001

2N5172

2N5172

Q_{99}

Q_{98}

Q_{97}

Q_{96}

C_{95} .01µF

CR_{47}

R_{216} 1K

R_{215} 301Ω

R_{217} 30Ω

L_{15} BEAD

L_{16} BEAD

CR_{45}

R_{201} 5.1Ω

R_{202} 475Ω

Q_{92} MPS 3640

R_{206} 15Ω

C_{98} .01µF

R_{207} 5Ω

R_{208} 6.19Ω

Q_{94} MPS 3640

Q_{93}

R_{209} 5.1Ω

CR_{46}

R_{210} 475Ω

"C" OUT

"D" OUT

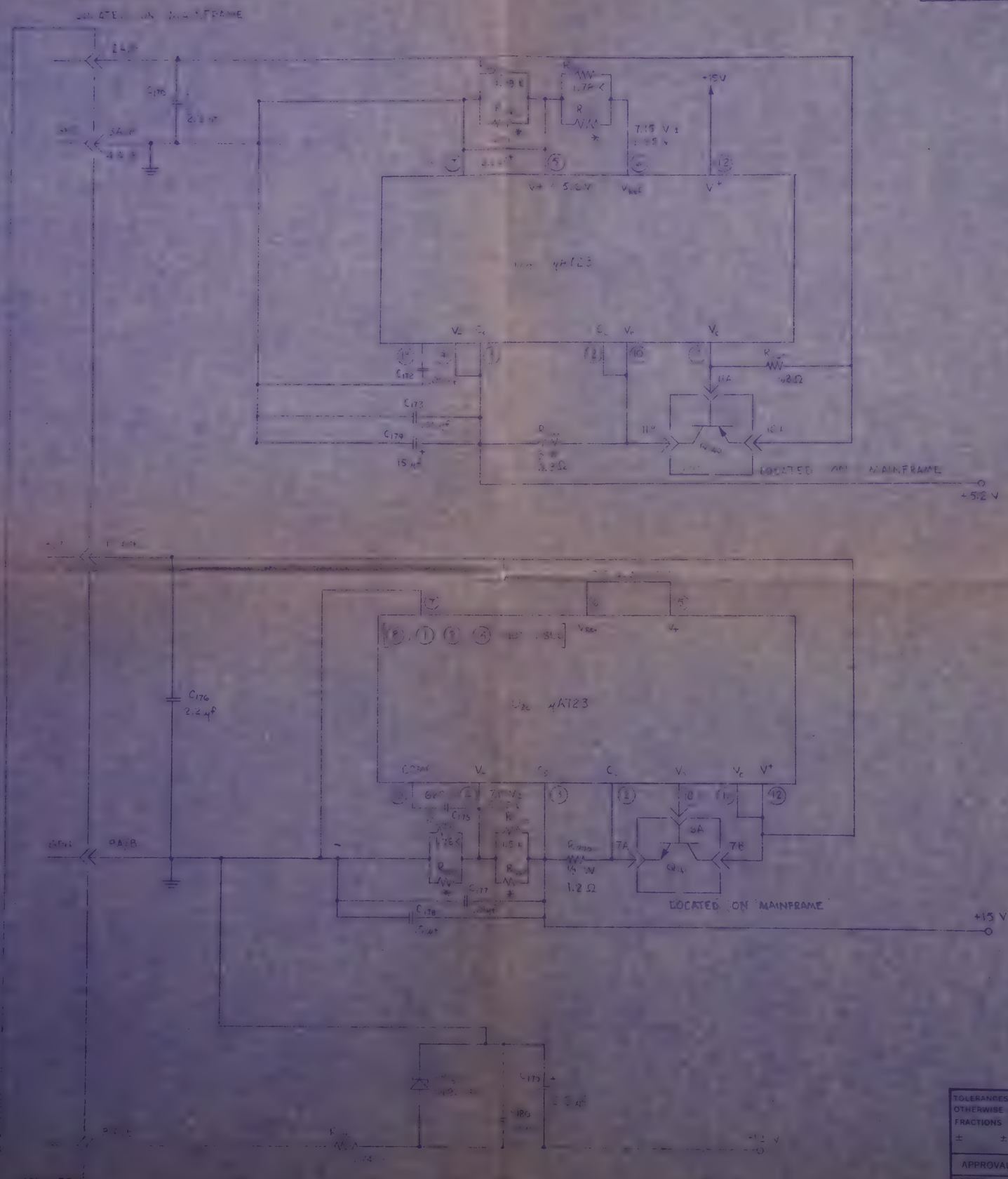
LOCATED ON MAINFRAME

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		PULSE INSTRUMENTS CO. SAN PEDRO, CALIFORNIA 90732	
APPROVALS	DATE	PLUGIN 4 CHANNEL CLOCK GENERATOR	
DRAWN	12/27/78	TTL TRANSLATOR	
CHECKED		SCALE	SIZE C / DRAWING NO.
		DO NOT SCALE DRAWING	SHEET

REPRODUCTION PROHIBITED

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	CHANGES IN R_{260}, R_{266}, R_{270}, U_{12}, U_{13}.	4-7-75	
B	CHANGES IN ALL CAPACITOR NUMBERS.	11-4-75	



NOTES: 1. * INDICATES SELECTED RESISTOR VALUE

TOLERANCES UNLESS OTHERWISE SPECIFIED	
FRACTIONS ±	DEC ±
ANGLES ±	

APPROVALS	DATE
DRAWN	
CHECKED	

PULSE INSTRUMENTS CO.
SAN PEDRO, CALIFORNIA 90732

PI 1004 4 CHANNEL CLOCK GENERATOR
POWER SUPPLIES

SCALE	SIZE	DRAWING NO.
	C	

DO NOT SCALE DRAWING | SHEET

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	NOTE 2. VALUE CHANGES AT R_4, C_{16}, C_{25}, C_{11}, C_{28}, C_{17}, C_{36}, L_2, L_5,	6-12-78	DK
B	VALUE CHANGES AT R_{10}, R_{18}, R_{48}, C_{11},	10-30-78	
C	TOOK OUT R_{54} 121K.	10-30-78	
D	VALUE CHANGES AT R_{35}, R_{36},	2-9-79	
E	ADDED VALUES AT U_1, U_3, U_4, U_5	2-15-79	

MASTER CLOCK "A"

"A" WIDTH GENERATOR

"B" DELAY GENERATOR

"B" WIDTH GENERATOR

NOTES: 1. ALL CR ARE IN914 UNLESS OTHERWISE SPECIFIED.
2. * DENOTES SELECTED VALUE.

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN MARINKOVICH	1/25/78
CHECKED	

PULSE INSTRUMENTS CO.
SAN PEDRO, CALIFORNIA 90732

PI-100 A 4 CHANNEL CLOCK GENERATOR
MASTER CLOCK "A", "B" DELAY GENERATOR
"A" AND "B" WIDTH GENERATORS

SCALE	SIZE	DRAWING NO.
	C	92000130

DO NOT SCALE DRAWING — SHEET 1 OF 5

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